REMARKS

Summary of Office Action

Claims 2-3 stand provisionally rejected under the judicially created doctrine of obviousness-type double patenting as allegedly being unpatentable over claims 1 and 3 of co-pending Application No. 10/025,906.

Claims 2, 3, 11, 12, and 18-22 stand rejected under 35 U.S.C. §102(e) as allegedly being anticipated by Nose et al. (US Pat. No. 6,819,311).

Claims 5-10 and 13-17 stand allowed.

Summary of Amendment

Claims 11 and 18 have been amended. No new matter has been entered. Claims 2, 3, 5-22 are currently pending for further consideration.

Allowed Claims

Applicants wish to thank the Examiner for allowance of claims 5-10 and 13-17. Based on the comments below, Applicants respectfully submit that the other pending claims (i.e., claims 2, 3, 11, 12, and 18-22) are also in condition for allowance.

All Claims Comply With §102

Claims 2, 3, 11, 12, and 18-22 stand rejected under 35 U.S.C. §102(e) as allegedly being anticipated by Nose et al. (US Pat. No. 6,819,311). Applicants respectfully traverse this rejection based on the following reasons.

Nose et al. only applies ***one*** gate output enable signal (OE). For instance, FIGs. 11-19 of Nose et al. teach that only ***one*** gate output enable signal (OE) is applied ***simultaneously*** to all

the gate drivers 11-14. Embodiment shown in FIG. 13 teaches that all of the OE inputs are commonly grounded. Embodiments shown in FIGs. 11, 15, 18, and 19 teach that two of the four gate drivers have an inverter stage coupled to the input. When the same output enable signal is applied to all four gates, the gates with the inverter stages receive an inverted signal OE-. This is verified when looking at the timing diagram shown in FIGs. 12, 16, and 17. Each of these timing diagrams shows that OE and OE- occur simultaneously, which means there is ***only one*** gate output enable signal being applied.

In contrast, independent claims 2 and 3, as previously presented, recite a method of driving a liquid crystal display including, in part, the step of "applying ***first to third*** gate output enable signals to the gate driver (emphasis added)." It is well settled that "[a] claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros. v. Union Oil Co. of California*. 814 F.2d 628, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). See also M.P.E.P. §2131. Since Nose et al. does not teach "applying first to third gate output enable signals" to the gate driver (i.e., Nose et al. applies only ***one*** enable signal (OE)), Applicants respectfully assert that Nose et al. does not anticipate claims 2 and 3 for at least this reason. Hence, Applicants respectfully request that the rejection be withdrawn.

Claim 11, as amended, recite, in part, a step of "displaying a specific dummy picture on the liquid crystal display panel on which said first picture has been displayed, wherein the specific dummy picture is ***selected based on one of first to third gate output enable signals***, and displaying a second picture over said specific dummy picture in a next frame, wherein the

second picture is ***selected based on another one of first to third gate output enable signals*** (emphasis added)." In contrast, Nose et al. teaches applying only one gate output enable signal (OE) as explained above. Hence, Nose et al. does not teach the step of displaying a specific dummy picture where the specific dummy picture is "selected based on one of first to third gate output enable signals" as recited in claim 11. For at least this reason, Nose et al. does not anticipate claim 11, and thus its dependent claim 12. Applicants therefore respectfully request that the rejection be withdrawn.

Claim 18, as amended, recites, in part, a step of "***selecting*** two gate lines that are separated by a predetermined number of gate lines ***based on received first to third gate output enable signals*** (emphasis added)." In contrast, Nose et al. teaches applying only one gate output enable signal (OE) used to select which picture is displayed as explained above. Hence, for at least this reason, Nose et al. does not anticipate claim 18, and thus its dependent claims 19-22. Applicants therefore respectfully request that the rejection be withdrawn.

Additionally, Applicants respectfully submit that Nose et al. does not disclose the "method steps" as recited in the claims. At best, Nose et al. discloses an "apparatus" that the Office Action asserts as performing the claimed method steps. However, because the circuit of Nose et al. has ***only one enable signal*** as discussed above, the method as recited in the present application cannot be applied using Nose et al.'s circuitry to properly drive an LCD panel. Therefore, Applicants respectfully assert that the circuit of Nose et al. does not and cannot perform the method steps as recited in the present application.

Provisional Obviousness-Type Double Patenting Rejection

Claims 2-3 stand provisionally rejected under the judicially created doctrine of obviousness-type double patenting as allegedly being unpatentable over claims 1 and 3 of co-pending Application No. 10/025,906. Applicants respectfully traverse this rejection for the following reasons.

Firstly, the asserted rejection appears improper because the analysis is based on the wrong claims. For instance, claims 2-3 of the present application was allegedly rejected. However, the claim chart comparing the claims of the present application to that of the co-pending application analyzes claims 1 and 2 of the present application to that of claims 1 and 3 of the co-pending application. It is reminded that claim 1 has previously been cancelled.

Secondly, the Office Action acknowledges that the co-pending application does not claim "applying first to third date output enable signals" but concludes that it would have been obvious to one of ordinary skill in the art at the time of the invention was made "to obtain applying first to third gate output enable signals to the gate driver in order to control output of gate driver and to improve the image quality." This "conclusion" is not based on any teachings or suggestions in the prior art as there is no teaching that would motivate one of ordinary skill to "apply first to third gate output enable signals to the gate driver" to the alleged claims of the co-pending application. The closest prior art as currently applied to the claims (Nose et al.) teaches applying ***only one*** gate output enable signal to improve picture quality as discussed above. Therefore, there is no *prima facie* case of obviousness to show that claims 2 and 3 of the present application is unpatentable over claims 1 and 3 of the co-pending application.

Though the obviousness-type double patenting rejection is only provisional as the co-pending application has not yet been patented, Applicants respectfully assert that the rejection should nevertheless be withdrawn for the reasons stated above.

CONCLUSION

In view of the foregoing, reconsideration and timely allowance of the pending claims are respectfully requested. Should the Examiner feel that there are any issues outstanding after consideration of the response, the Examiner is invited to contact the Applicants' undersigned representative to expedite prosecution.

If there are any other fees due in connection with the filing of this response, please charge the fees to our Deposit Account No. 50-0310. If a fee is required for an extension of time under 37 C.F.R. 1.136 not accounted for above, such an extension is requested and the fee should also be charged to our Deposit Account.

Respectfully submitted,

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